



We wanted to make sure that you will benefit from one of Concept Engineering's EDA tools this spring. Tools for debugging and verification!

Evaluation is simple and free. Try us!

KAL - Large IP Cores:

CPU Cores:

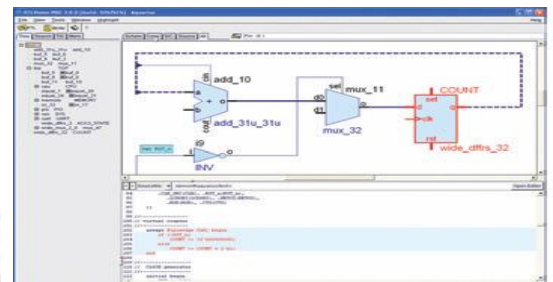
- 8 bit - 8051
- 8 bit- HC68HC11
- 8 bit - PIC Processor
- 8 bit – Z80
- 16 bit – D6800
- DSP – MSP430
- 32 bit - ARM 9xx/11xx

Memory Controllers:

- SD/SDIO 2.0/3.0 Controller
- SDRAM Controller
- DDR/DDR2/DDR3 SDRAM Controller
- NAND Flash Controller
- Flash/EEPROM/SRAM Controller
- PCMCIA/CompactFlash Host Adapter
- PCMCIA/CompactFlash Slave Controller

Clock Synchronization:

- IEEE 1588 Slave
- IEEE 1588 Master
- IEEE 1588 Master/Slave
- IEEE 1588 PTP Stack



RTLvision[®]PRO provides engineers with the ability to easily understand, debug and optimize RTL code (e.g., third party IP). RTLvision PRO helps to reduce the complexity of the debug process via its interactive logic cone navigation feature, showing just the critical portion of the RTL design in the logic cone window while providing links to the original RTL source code at the same time. The tool provides mixed language support for System Verilog, Verilog and VHDL, and ultra fast HDL readers.

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- IEEE 1588 L2/L3 Solution

Peripherals:

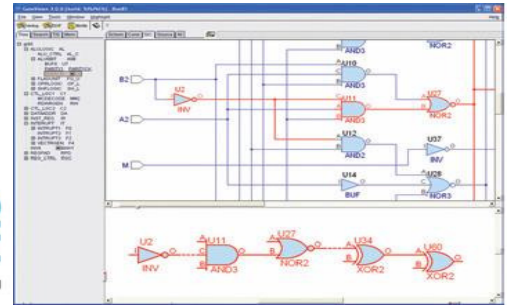
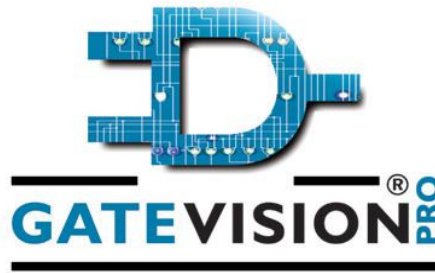
- Floating Point Unit
- I2C Master/Slave
- SPI Master/Slave
- CAN bus
- LIN bus
- Programmable Peripheral Interface
- UART, UART with FIFO
- PWM
- Timer 8254
- Programmable Timer
- Interrupt Controller
- Ethernet Controller 10/100/1000 BaseT
- DMA Controller
- USB 1.0/2.0 Host/Slave
- On Chip Bus Analyzer

PCI Bus Controllers and Peripherals:

- PCI Express
- PCI-X Host Bridge Master/Target
- PCI Host Bridge Master/Target
- PCI-PCI Bridge
- PCI-ISA Bridge
- PCI Bus Arbiter

Memory Library:

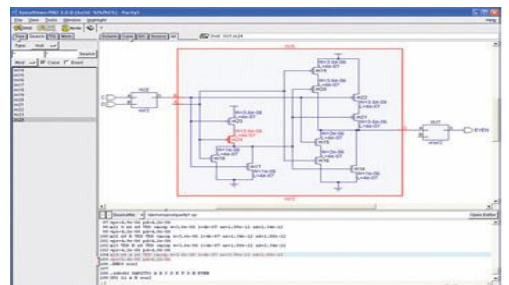
- CAM
- Low Power SRAM Solutions
- Low Power Register Files
- Low Power ROM
- Custom per customer need



GateVision® PRO is an extreme performance gate-level debugger that allows intuitive design navigation, logic cone extraction, interactive logic cone viewing, and design documentation. GateVision PRO supports standards such as Verilog, EDIF or LEF/DEF. GateVision PRO's unique cone features facilitate interactive navigation within just that portion of the circuit that is most important for the job at hand. A Tcl-based UserWare API enables customers to write their own specific functions (e.g., company specific ERC).

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SpiceVision® PRO is a transistor level debugger and fits into any design flow where SPICE design files (CDL, Calibre, HSPICE, DSPF, ELDO, PSPICE, SPICE) are used to verify circuit behavior. It produces easy-to-read transistor level schematics from complex SPICE descriptions, helps engineers to visualize parasitic effects within deep-submicron designs and reduces the design and debug time for engineers who work at the SPICE netlist level. A UserWare API provides compelling flexibility for customization.

Encryption:

- AES 128bit/256bit
- ECC

AHB/APB Peripherals:

- AHB Bus Master/Slave
- APB Bus Master/Slave
- AHB/AXI DMA Controller
- AXI Bus Master/Slave

MIPS CPU Interface:

- MIPS - SysAD Bus Slave
- MIPS - SysAD Bus to PCI Host bridge
- MIPS - EC interface to SDRAM Controller
- MIPS - EC Interface to PCI Host Bridge
- MIPS - EC Interface Bus Slave

PowerPC CPU Interface:

- Power PC Bus Master
- PowerPC to PCI Host bridge
- PowerPC Bus Arbiter
- PowerPC Bus Slave

ARC CPU Interface:

- ARC - Peripheral Controller for ARCTangent
- ARC – ARCTangent to PCI host Bridge

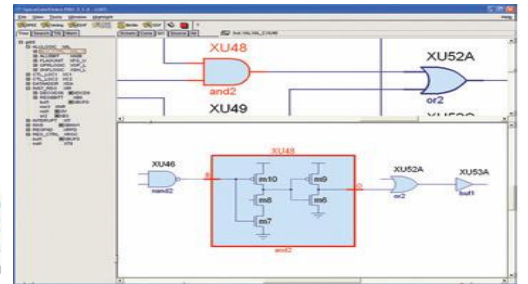
Analog IP Cores:

- Analog IP cores (ADC, DAC, PLL,) are available – Please contact us.
- We are expert in custom analog IP

[Contact us for data sheet](#)

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SGvision™PRO is a debugging tool that analyzes mixed-level descriptions in a single tool. Both top level structures described in Verilog and lower level structures described via SPICE can be debugged in an integrated environment. With SGvision PRO, it is possible to see schematics and traverse the signal flow of gates as well as transistors in the same window, improving understanding of the circuits and accelerating debugging. A powerful tcl-based UserWare API allows tool customization.

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