



We are pleased to provide you with the latest news from our partners. We have a lot of customers like

Until then, we thank you for your continued support!

Large IP Cores:

CPU Cores:

- 8 bit - 8051
- 8 bit- HC68HC11
- 8 bit - PIC Processor
- 8 bit – Z80
- 16 bit – D6800

• DSP – MSP430

- 32 bit - ARM 9xx/11xx

Memory Controllers:

- SD/SDIO 2.0/3.0 Controller
- SDRAM Controller
- DDR/DDR2/DDR3 SDRAM Controller
- NAND Flash Controller
- Flash/EEPROM/SRAM Controller
- PCMCIA/CompactFlash Host Adapter
- PCMCIA/CompactFlash Slave Controller

Clock Synchronization:

- IEEE 1588 Slave
- IEEE 1588 Master
- IEEE 1588 Master/Slave
- IEEE 1588 PTP Stack
- IEEE 1588 L2/L3 Solution

Flash/ROM/SRAM Controller IP Core- Short Overview

The Flash/ROM/SRAM controller core allows two or more access ports to share memory access to the FLASH, ROM and SRAM devices. The core automatically arbitrates between the two access ports so each can access memory independently.

Benefits

- Proven on Silicon & Standard based.
- Low Risk and support for years.
- Changes/adaptation per customer request in short time 2 market to lower the gate count and add host ports.

Features

- Supports industry standard Asynchronous SRAM, NOR Flash, ROM and similar memory devices.
 - Two request ports to allow two requesters to share access to the FLASH/ROM/SRAM devices.
 - 8 Chip select signals to access up to 8 memory banks.
 - Independent programmable timing parameters for each chip select.
 - Independent address mapping for each chip select.

Peripherals:

- Floating Point Unit
- I2C Master/Slave
- SPI Master/Slave
- CAN bus
- LIN bus
- Programmable Peripheral Interface
- UART, UART with FIFO
- PWM
- Timer 8254
- Programmable Timer
- Interrupt Controller
- Ethernet Controller 10/100/1000 BaseT
- DMA Controller
- USB 1.0/2.0 Host/Slave
- On Chip Bus Analyzer

PCI Bus Controllers and Peripherals:

- PCI Express
- PCI-X Host Bridge Master/Target
- PCI Host Bridge Master/Target
- PCI-PCI Bridge
- PCI-ISA Bridge
- PCI Bus Arbiter

Memory Library:

- CAM
- Low Power SRAM Solutions
- Low Power Register Files
- Low Power ROM
- Custom per customer need

Encryption:

- Independent programmable data width of 8, 16 and 32 bits for each chip select.
- Supports 32-bit and 64-bit user interface bus width.
- Supports burst access from the request ports.
- Automatic issues multiple access to memory device (byte collection) to match data word size of memory device with user interface data width.
- Optional AHB/AXI user interface.
- Optional ECC protection.
- Optimized for logic synthesis for ASIC and FPGA implementations.
- Fully static design with edge triggered flip-flops.

[Block Diagram- click here](#)

About Eureka Technology

[Eureka Technology Inc.](#) is a leading intellectual property (IP) provider for ASIC, FPGA and system designers. The company specializes in the integration and customization of standard IP core to meet customer requirements.

Eureka offers a wide range of silicon proven system core logic and peripheral function cores for different CPU and bus standards including PowerPC™, AHB™, AXI™, PCI™, PCI-X™, PCI Express™, Cardbus™, SDR/DDR SDRAM, NAND Flash, Secure Digital (SD™), MMC, CompactFlash™ and PCMCIA™.

These IP cores are designed to improve the design time-to-market, eliminate design risks, and reduce development costs for System-on-chip (SoC) designs. Located in Silicon Valley, California, Eureka Technology has pioneered the use of IP cores as a standard methodology in IC design and has licensed hundreds of IP cores to many leading companies in the semiconductor and electronic industries.

With customer base in the US, Europe, Japan and other parts of Asia, the company has built many long term business relationships with its customers after their initial successes.

- AES 128bit/256bit
- ECC

AHB/APB Peripherals:

- AHB Bus Master/Slave
- APB Bus Master/Slave
- AHB/AXI DMA Controller
- AXI Bus Master/Slave

MIPS CPU Interface:

- MIPS - SysAD Bus Slave
- MIPS - SysAD Bus to PCI Host bridge
- MIPS - EC interface to SDRAM Controller
- MIPS - EC Interface to PCI Host Bridge
- MIPS - EC Interface Bus Slave

PowerPC CPU Interface:

- Power PC Bus Master
- PowerPC to PCI Host bridge
- PowerPC Bus Arbiter
- PowerPC Bus Slave

ARC CPU Interface:

- ARC - Peripheral Controller for ARCTangent
- ARC – ARCTangent to PCI host Bridge

Analog IP Cores:

- Analog IP cores (ADC, DAC, PLL,) are available – Please contact us.
- We are expert in custom analog IP

[Contact us for data sheet](#)

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