eNewsletter

KAL - Large IP Cores:

Analog IP Cores:

- **DDR2/3 PHY**
- **Analog IP cores (ADC, DAC, PLL,) are available – Please contact us.**
- **We are expert in custom analog IP**

CPU Cores:

- **8 bit - 8051**
- **8 bit- HC68HC11**
- **8 bit - PIC Processor**
- **8 bit – Z80**
- **16 bit – D6800**
- **DSP – MSP430**
- **32 bit - ARM 9xx/11xx**

Memory Controllers:

- **SD/SDIO 2.0/3.0 Controller**
- **SDRAM Controller**
- **DDR/DDR2/DDR3 SDRAM Controller**
- **NAND Flash Controller**
- **Flash/EEPROM/SRAM Controller**
- **PCMCIA/CompactFlash Host Adapter**
- **PCMCIA/CompactFlash Slave Controller**

Clock Synchronization:

- **IEEE 1588 Slave**
- **IEEE 1588 Master**

News form our ASIC EDA tool partner - Concept Engineering Introduces Integrated Debugging Tool for Mixed-signal Design at DAC 2011

StarVision™ PRO works at different design levels, with different design languages and netlist formats, for easy debugging and analysis of SoCs and ICs

Design and verification engineers who work on complex analog/mixedsignal (AMS) designs or who need to customize and integrate analog or digital IP building blocks into their system-on-chip (SoC) or integrated circuit (IC) designs will be able to assess a new analysis and debugging tool at DAC 2011. Due to the increasing use of building blocks in SoC design, engineers need to work at different design levels (RTL, gate, transistor, analog, etc.) as well as with different design languages and netlist formats. To support this challenge, Concept Engineering developed StarVision PRO, an integrated debugging cockpit for AMS and digital design that makes analysis and debugging of complex SoC and IC designs easy and more transparent.

“Increasingly, complex design requires design and verification engineers to integrate and understand design building blocks from different sources and on different design levels,” said Gerhard Angst, CEO and president of Concept Engineering. “In response to this challenge faced by so many customers, we built StarVision PRO precisely to provide a way to manage these different languages and design levels at the same time in the same integrated tool.” StarVision PRO provides engineers with the ability to quickly and easily understand and debug mixed-mode designs and to customize and integrate IP building blocks into their complex SoCs and ICs. A combination of Concept Engineering’s successful tools for RTL-, gate-, and transistor-level debugging (RTLvision® PRO, GateVision® PRO and SpiceVision® PRO), StarVision PRO provides full visibility and control over design data in one integrated debugging cockpit for designs that contain blocks defined at various levels, allowing analysis and debug of circuits with both digital and transistor-level components at the same time. StarVision

- **IEEE 1588 Master/Salve**
- **IEEE 1588 PTP Stack**
- **IEEE 1588 L2/L3 Solution**

Peripherals:

- **Floating Point Unit**
- **I2C Master/Slave**
- **SPI Master/Slave**
- **CAN bus**
- **LIN bus**
- **Programmable Peripheral Interface**
- **UART, UART with FIFO**
- **PWM**
- **Timer 8254**
- **Programmable Timer**
- **Interrupt Controller**
- **Ethernet Controller 10/100/1000 BaseT**
- **DMA Controller**
- **USB 1.0/2.0 Host/Salve**
- **On Chip Bus Analyzer**

PCI Bus Controllers and Peripherals:

- **PCI Express**
- **PCI-X Host Bridge Master/Target**
- **PCI Host Bridge Master/Target**
- **PCI-PCI Bridge**
- **PCI-ISA Bridge**
- **PCI Bus Arbiter**

Encryption:

- **AES 128bit/256bit**
- **ECC**

AHB/APB Peripherals:

- **AHB Bus Master/Slave**

PRO supports all important RTL, netlist and transistor-level languages: Verilog, SystemVerilog, VHDL, SPICE, HSPICE, ELDO, DSPF, EDIF and more.

Waveform Viewer and Signal Tracing

As well as providing easy signal tracing at different design levels and for different languages, with faster problem exploration and better visibility into IP building blocks, StarVision PRO also comes with a fully integrated waveform viewer and with support for interactive signal tracing in the source code, schematic view and waveform window. StarVision PRO compiles VCD simulation data into its own high-speed format for accelerated waveform browsing and signal tracing.

Fragment Navigation

StarVision PRO reduces the complexity of the debug process via its interactive logic cone navigation window, showing schematic fragments of just the critical portion of the design in the logic cone window while providing links to the original source code and simulation results at the same time. As a result, engineers can work easily on the important critical circuit fragments of their designs and are not disturbed by graphics and information that is not relevant for the job at hand. Visual feedback about important elements of the design (RTL, gates, transistors, parasitic elements) helps users to understand and solve the current design/verification problem.

Customization

StarVision PRO is very easy to use, with very high performance and high capacity. A tcl-based UserWare API provides flexible customization and allows access to the internal database and graphical user interface (GUI).Users can analyze the design data and generate company-specific and project-specific design reports and electrical design rule checks (user-defined ERCs).

About Concept Engineering

Concept Engineering is a privately held company based in Freiburg, Germany, founded in 1990 to develop and market innovative automatic schematic generation and viewing technology for use with logic synthesis, verification, test automation and physical design tools. The company's customers are primarily original equipment EDA tool manufacturers (OEMs), in-house CAD tool developers and semiconductor companies.

- **APB Bus Master/Slave**
- **AHB/AXI DMA Controller**
- **AXI Bus Master/Slave**

MIPS CPU Interface:

- **MIPS - SysAD Bus Slave**
- **MIPS - SysAD Bus to PCI Host bridge**
- **MIPS - EC interface to SDRAM Controller**
- **MIPS - EC Interface to PCI Host Bridge**
- **MIPS - EC Interface Bus Slave**

PowerPC CPU Interface:

- **Power PC Bus Master**
- **PowerPC to PCI Host bridge**
- **PowerPC Bus Arbiter**
- **PowerPC Bus Slave**

ARC CPU Interface:

- **ARC - Peripheral Controller for ARCtangent**
- **ARC – ARCtangent to PCI host Bridge**

Contact us for data sheet

For more information, see http://www.concept.de.

Contact us for more information.

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Untill the next eNews,

Thanks yu for your attenstion.

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