eNewsletter

KAL - Large IP Cores:

Analog IP Cores:

- Analog IP cores (ADC, DAC, PLL,) are available – Please contact us.
- We are expert in custom analog IP

CPU Cores:

- 8 bit - 8051
- 8 bit- HC68HC11
- 8 bit - PIC Processor
- 8 bit – Z80
- 16 bit – D6800
- DSP – MSP430

Memory Controllers:

- SD/SDIO 2.0/3.0 Controller
- SDRAM Controller
- DDR/DDR2/DDR3 SDRAM Controller
- NAND Flash Controller
- Flash/EEPROM/SRAM Controller
- PCMCIA/CompactFlash Host Adapter
- PCMCIA/CompactFlash Slave Controller

Clock Synchronization:

- IEEE 1588 Slave
- IEEE 1588 Master
- IEEE 1588 Master/Salve
- IEEE 1588 PTP Stack

Programmable Interrupt Controller D8259 from Digital Core Design

Digital Core Design, IP Core provider and the System on Chip design house from Poland introduced in its offer the D8259. DCD's Programmable Interrupt Controller is fully compatible with the 82C59A device. As all other cores design by Polish company, the D8259 is tech-nology independent, so it can be implemented both in ASIC and FPGA.

The D8259 is a soft Core of Programmable Interrupt Controller, which is fully compatible with the 82C59A device. DCD's IP core can manage up to 8-vectored priority interrupts for the processor. – ***But that's not all, cause you can also program it to cascade and gain up to 64 vectored interrupts*** - adds Jacek Hanke, DCD's CEO. And if it still seems to be not enough, one can always get more than 64 vectored interrupts, by programming the D8259 to the Poll Command Mode.

The D8259 Package includes fully automated testbench. Thanks to complete set of tests, one can easily validate the whole package at each stage of SoC design flow. Same as all other DCD's IP Cores, this one's got also a technology independent design, that can be implemented in a variety of process technologies.
The D8259 can operate in all 82C59A modes and it supports all 82C59A features:

- MCS80/85 and 8088/8086 processor modes
  - Fully nested mode and special fully nested mode
  - Special mask mode

- **IEEE 1588 L2/L3 Solution**

Peripherals:

- **Floating Point Unit**
- **I2C Master/Slave**
- **SPI Master/Slave**
- **CAN bus**
- **LIN bus**
- **Programmable Peripheral Interface**
- **UART, UART with FIFO**
- **PWM**
- **Timer 8254**
- **Programmable Timer**
- **Interrupt Controller**
- **Ethernet Controller 10/100/1000 BaseT**
- **DMA Controller**
- **USB 1.0/2.0 Host/Salve**
- **On Chip Bus Analyzer**

PCI Bus Controllers and Peripherals:

- **PCI Express**
- **PCI-X Host Bridge Master/Target**
- **PCI Host Bridge Master/Target**
- **PCI-PCI Bridge**
- **PCI-ISA Bridge**
- **PCI Bus Arbiter**

Encryption:

- **AES 128bit/256bit**
- **ECC**

AHB/APB Peripherals:

- **AHB Bus Master/Slave**
- **APB Bus Master/Slave**
- **AHB/AXI DMA Controller**

- Buffered mode
- Pool command mode
- Cascade mode with master or slave selection
- Automatic end of interrupt mode
- Specific and non specific end of interrupt commands
- Automatic and Specific Rotation
- Edge and level triggered interrupt input modes
- Reading of interrupt request register (IIR) and in service register (ISR) through data bus.
- Writing and reading of interrupt mask register (IMR) through data bus

Contact us for more information.

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Until the next eNews,

Thanks you for your attention.

KAL

- **AXI Bus Master/Slave**

MIPS CPU Interface:

- **MIPS - SysAD Bus Slave**
- **MIPS - SysAD Bus to PCI Host bridge**
- **MIPS - EC interface to SDRAM Controller**
- **MIPS - EC Interface to PCI Host Bridge**
- **MIPS - EC Interface Bus Slave**

PowerPC CPU Interface:

- **Power PC Bus Master**
- **PowerPC to PCI Host bridge**
- **PowerPC Bus Arbiter**
- **PowerPC Bus Slave**

ARC CPU Interface:

- **ARC - Peripheral Controller for ARCtangent**
- **ARC – ARCtangent to PCI host Bridge**

Contact us for data sheet

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