



KAL - Large IP Cores:

Analog IP Cores:

- Analog IP cores (ADC, DAC, PLL,) are available – Please contact us.
- We are expert in custom analog IP

CPU Cores:

- 8 bit - 8051
- 8 bit- HC68HC11
- 8 bit - PIC Processor
- 8 bit – Z80
- 16 bit – D6800
- DSP – MSP430
- 32 bit - ARM 9xx/11xx

Memory Controllers:

- SD/SDIO 2.0/3.0 Controller
- SDRAM Controller
- DDR/DDR2/DDR3 SDRAM Controller
- NAND Flash Controller
- Flash/EEPROM/SRAM Controller
- PCMCIA/CompactFlash Host Adapter
- PCMCIA/CompactFlash Slave Controller

Clock Synchronization:

- IEEE 1588 Slave
- IEEE 1588 Master
- IEEE 1588 Master/Slave
- IEEE 1588 PTP Stack

NEW IP Core by MAZ Brandenburg GmbH - MSP430 compatible 16bit DSP IP Core for ASIC/FPGA Design.

The DSP is proven on silicon and already in use in many designs for more than 2 years. The IP has software tools for embedded software development. We deliver the IP as RTL which allow you to use the DSP with any technology (FPGA or ASIC) and any silicon geometry or foundry with no EDA tools restriction.

This IP core is among the other state of the art IP core such as 8051, PIC and other processors, peripherals and memory controllers.

We provide the IPs with selected peripherals per the customer choice and can provide it with special design up to full chip.

MSP430 IP Core Features:

- Opcode compatible to TI's MSP430.
- Harvard architecture and AHBL data and instruction bus interfaces.
- RISC architecture with 27 instructions and 7 addressing modes.
- Orthogonal architecture: every instruction usable with every addressing mode.
- Full register access including program counter, status registers, and stack pointer.
- 16 x 16-bit register.
- 64 KByte linear address space.
- 16-bit native data bus width.
- Constant generator provides six most used immediate values and reduces code size.
- Direct memory-to-memory transfers without intermediate register holding.
- Word and byte addressing and instruction formats.
- Several C compilers are available.

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-> [Contact us](#) for more information:

by phone: 04-6201129 Ext 4

- IEEE 1588 L2/L3 Solution

Peripherals:

- Floating Point Unit
- I2C Master/Slave
- SPI Master/Slave
- CAN bus
- LIN bus
- Programmable Peripheral Interface
- UART, UART with FIFO
- PWM
- Timer 8254
- Programmable Timer
- Interrupt Controller
- Ethernet Controller
10/100/1000 BaseT
- DMA Controller
- USB 1.0/2.0 Host/Slave
- On Chip Bus Analyzer

PCI Bus Controllers and Peripherals:

- PCI Express
- PCI-X Host Bridge
Master/Target
- PCI Host Bridge
Master/Target
- PCI-PCI Bridge
- PCI-ISA Bridge
- PCI Bus Arbiter

Encryption:

- AES 128bit/256bit
- ECC

AHB/APB Peripherals:

- AHB Bus Master/Slave
- APB Bus Master/Slave
- AHB/AXI DMA Controller

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Untill the next eNews,

Thanks yu for your attenstion.

KAL

- AXI Bus Master/Slave

MIPS CPU Interface:

- MIPS - SysAD Bus Slave
- MIPS - SysAD Bus to PCI Host bridge
- MIPS - EC interface to SDRAM Controller
- MIPS - EC Interface to PCI Host Bridge
- MIPS - EC Interface Bus Slave

PowerPC CPU Interface:

- Power PC Bus Master
- PowerPC to PCI Host bridge
- PowerPC Bus Arbiter
- PowerPC Bus Slave

ARC CPU Interface:

- ARC - Peripheral Controller for ARCTangent
- ARC – ARCTangent to PCI host Bridge

[Contact us for data sheet](#)

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