

**KAL - Large IP Cores:**

Memory Controllers:

- **SD/SDIO 2.0/3.0 Controller**
- SDRAM Controller
- **DDR/DDR2/DDR3 SDRAM Controller**
- NAND Flash Controller
- Flash/EEPROM/SRAM Controller
- PCMCIA/CompactFlash Host Adapter
- PCMCIA/CompactFlash Slave Controller

CPU Cores:

- **32 bit - NEW**
- **8 bit - 8051**
- 8 bit- HC68HC11
- 8 bit - PIC Processor
- 8 bit - Z80
- 16 bit - D6800

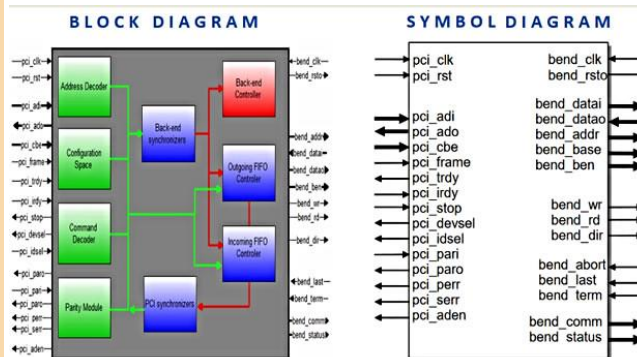
Clock Synchronization:

- IEEE 1588 Slave
- IEEE 1588 Master
- IEEE 1588 Master/Slave
- IEEE 1588 PTP Stack
- IEEE 1588 L2/L3 Solution

Peripherals:

- HDLC/SDLC
- Smart Card Reader Unit
- EEPROM SPI Ctrl
- LCD Ctrl
- Floating Point Unit
- I2C Master/Slave

## IP builds dual clock 32bit PCI Bus target interface



*Digital Core Design adds the DTPCI32DC, a dual clock 32-bit PCI bus target interface IP Core which meets all requirements of the PCI 3.0 specification for a target device: the IP uses a minimal gate count with a high-bandwidth data transfer.*

The core's main feature is the presence of two clock domains, for flexibility and higher performance; its user-friendly back-end

- SPI Master/Slave
- CAN bus
- LIN bus
- Programmable Peripheral Interface
- UART, UART with FIFO
- PWM
- Timer 8254
- Programmable Timer
- Interrupt Controller
- Ethernet Controller 10/100/1000 BaseT
- DMA Controller
- USB 1.0/2.0 Host/Slave
- On Chip Bus Analyzer

#### PCI Bus Controllers and Peripherals:

- PCI Express
- PCI-X Host Bridge Master/Target
- PCI Host Bridge Master/Target
- PCI-PCI Bridge
- PCI-ISA Bridge
- PCI Bus Arbiter

#### Modulation:

- ADPSM

#### AHB/APB Peripherals:

- AHB Bus Master/Slave
- APB Bus Master/Slave
- AHB/AXI DMA Controller
- AXI Bus Master/Slave

#### Analog IP Cores:

- Analog IP cores (ADC, DAC, PLL,) are available – Please contact us.
- We are expert in custom analog IP

[Contact us for data sheet](#)

interface can be very easily and effectively tailored to the design needs. The Core supports up to six base address registers and expansion ROM address register with both I/O and memory space decoding from 16 Bytes up to 4 GB. Another important feature is a cache wrapping hardware support and a cacheline pre-fetching capability. The DTPCI32DC accepts size cache lines which are powered from 2 up to 128. It enables also target-disconnect with data, without data or by a target abort. The core is capable of working at 66 MHz clock frequency in the most popular technologies. It assures the PCI timing requirements, as well as other parameters such as FIFO depths number or base address registers which can be configured at the pre-synthesis stage.

#### Features include:

- Fully supports PCI specification 3.0 protocol
- Stable clock domain crossing regardless of the

clock frequencies

- Cache wrapping (cache lines must be powers of 2)
- User controlled burst data transfer
- Possible no-wait state transactions
- Automatic handling of configuration space read/write access
- Parity generation and parity error detection
- Single interrupt support
- Configurable FIFOs depth
- Supported backend initiated burst termination (with and without data)
- No tri-state buffers

More information:

<http://dcd.pl/ipcore/1112/dtpci32dc/>

KAL is representing DCD.

[www.dcd.pl](http://www.dcd.pl)

[www.KALtech.co.il](http://www.KALtech.co.il)

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We are looking forward to hear from you.  
Contact us for more information.

Tel +972-77-7199944

<http://www.KALtech.co.il>  
[info@kaltech.co.il](mailto:info@kaltech.co.il)

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Until the next eNews,

Thanks you for your attention.

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