eNewsletter

KAL - Large IP Cores:

Analog IP Cores:

- **Analog IP cores (ADC, DAC, PLL,) are available – Please contact us.**
- **We are expert in custom analog IP**

CPU Cores:

- **8 bit - 8051**
- **8 bit- HC68HC11**
- **8 bit - PIC Processor**
- **8 bit – Z80**
- **16 bit – D6800**
- **DSP – MSP430**

Memory Controllers:

- **SD/SDIO 2.0/3.0 Controller**
- **SDRAM Controller**
- **DDR/DDR2/DDR3 SDRAM Controller**
- **NAND Flash Controller**
- **Flash/EEPROM/SRAM Controller**
- **PCMCIA/CompactFlash Host Adapter**
- **PCMCIA/CompactFlash Slave Controller**

Clock Synchronization:

- **IEEE 1588 Slave**
- **IEEE 1588 Master**
- **IEEE 1588 Master/Salve**
- **IEEE 1588 PTP Stack**
- **IEEE 1588 L2/L3 Solution**

Concept Engineering Adds SPEF Parasitic Netlist Interface to SpiceVision® PRO and StarVision® PRO

Concept Engineering has added a new SPEF (standard parasitic exchange format) interface to their widely-installed debugging tools, SpiceVision® PRO and StarVision® PRO. SpiceVision PRO takes SPICE netlists and SPICE models and generates clean, easy-to-read transistor-level schematics, circuit fragments, and design documentation to speed up circuit design, circuit debugging and circuit optimization at the transistor level. StarVision PRO, an integrated debugging cockpit for Mixed-Signal design, makes analysis and debugging of complex SoC (system on chip) and IC (integrated circuit) designs easy and more transparent.

Shrinking semiconductor process geometries and increased number of metal layers, interconnections and components create an enormous number of parasitic devices during netlist extraction and create a severe situation for simulation and signoff engineers. The new SPEF interface, and the already-available DSPF (Detailed Standard Parasitic Format) interface, give design engineers using SpiceVision PRO and StarVision PRO an easy way to analyze and explore parasitic structures in order to better understand, manage and optimize timing, signal integrity or IR-drop within their designs. The SPEF file format is an IEEE standard to define parasitic networks and contains precise information about interconnections and the related parasitic components.

Concept Engineering′s new SPEF interface provides engineers with very detailed information about the post-layout interconnections on their chips, allowing them to easily visualize and explore parasitic netlists and to precisely

Peripherals:

- Floating Point Unit
- I2C Master/Slave
- SPI Master/Slave
- CAN bus
- LIN bus
- Programmable Peripheral Interface
- UART, UART with FIFO
- PWM
- Timer 8254
- Programmable Timer
- Interrupt Controller
- Ethernet Controller 10/100/1000 BaseT
- DMA Controller
- USB 1.0/2.0 Host/Salve
- On Chip Bus Analyzer

PCI Bus Controllers and Peripherals:

- PCI Express
- PCI-X Host Bridge Master/Target
- PCI Host Bridge Master/Target
- PCI-PCI Bridge
- PCI-ISA Bridge
- PCI Bus Arbiter

Encryption:

- AES 128bit/256bit
- ECC

AHB/APB Peripherals:

- AHB Bus Master/Slave
- APB Bus Master/Slave
- AHB/AXI DMA Controller
- AXI Bus Master/Slave

locate and understand post-layout problems. In addition the new technology provides a very comfortable way to isolate and generate post-layout SPICE netlists of specific critical circuit fragments. Such isolated netlist fragments can then be used for fast and detailed circuit simulation and result in significantly accelerated post layout simulation.

"Concept Engineering is focused on providing design and verification engineers with the best possible ways to understand and analyze complex design descriptions from different sources, different design languages and on different design levels," said Gerhard Angst, CEO and president of Concept Engineering. "Now, with two dedicated interfaces available, customers will be able to more easily understand and manage extracted parasitic netlists and the impact of parasitic elements on their designs. The SPEF and DSPF interfaces provide users with a comfortable way to visualize and analyze the most important post-layout data formats of today's advanced design flows."

Pricing and availability

The SPEF interface for StarVision PRO is available at no additional cost. For SpiceVision PRO, the SPEF interface is available as part of the optional "Parasitic Analysis Package."

Contact us for more information or replay to this email.

About Concept Engineering

Concept Engineering is a privately held company based in Freiburg, Germany, founded in 1990 to develop and market innovative schematic generation and viewing technology for use with logic synthesis, verification, circuit characterization, circuit optimization, test automation and physical design

MIPS CPU Interface:

- **MIPS - SysAD Bus Slave**
- **MIPS - SysAD Bus to PCI Host bridge**
- **MIPS - EC interface to SDRAM Controller**
- **MIPS - EC Interface to PCI Host Bridge**
- **MIPS - EC Interface Bus Slave**

PowerPC CPU Interface:

- **Power PC Bus Master**
- **PowerPC to PCI Host bridge**
- **PowerPC Bus Arbiter**
- **PowerPC Bus Slave**

ARC CPU Interface:

- **ARC - Peripheral Controller for ARCtangent**
- **ARC – ARCtangent to PCI host Bridge**

Contact us for data sheet

tools. The company's customers are primarily EDA tool manufacturers (OEMs), in-house CAD tool developers and semiconductor companies. For more information see http://www.concept.de.

Contact us for more information.

Tel +972-4-6201129 Ext: 4

Fax +972-4-6201328

www.KALtech.co.il

info@kaltech.co.il

Facebook: kal silicon

Until the next eNews,

Thanks you for your attention.

KAL

Contact details:

Tel +972-4-6201129

Fax +972-4-6201328

www.KALtech.co.il

info@kaltech.co.il

eNews registration: http://www.kaltech.co.il/