eNewsletter

KAL - Large IP Cores:

Analog IP Cores:

- Analog IP cores (ADC, DAC, PLL,) are available – Please contact us.
- We are expert in custom analog IP

CPU Cores:

- 8 bit - 8051
- 8 bit- HC68HC11
- 8 bit - PIC Processor
- 8 bit – Z80
- 16 bit – D6800
- DSP – MSP430

Memory Controllers:

- SD/SDIO 2.0/3.0 Controller
- SDRAM Controller
- DDR/DDR2/DDR3 SDRAM Controller
- NAND Flash Controller
- Flash/EEPROM/SRAM Controller
- PCMCIA/CompactFlash Host Adapter
- PCMCIA/CompactFlash Slave Controller

Clock Synchronization:

- IEEE 1588 Slave
- IEEE 1588 Master
- IEEE 1588 Master/Salve
- IEEE 1588 PTP Stack
- IEEE 1588 L2/L3 Solution

DCD has released the D16950, which is an IP Core of a Uni-versal Asynchronous Receiver/Transmitter (UART), functionally compatible to the OX16C950. It allows serial transmission in two modes: UART and FIFO. In the FIFO mode, internal FIFOs are activated, allowing 128 bytes (plus 3 bits of error data per byte in the RCVR FIFO) to be stored in both receive and transmit modes.

DCD's UART IP Core performs a serial-to-parallel conversion on data characters received from a peripheral device or a MODEM. And for those who need more, the D16950 enables also parallel-to-serial conversion on data characters received from the CPU. The processor can read a complete status of the UART at any time during the functional operation. Reported status information includes the type and condition of transfer operations being performed by the UART, as well as any error conditions (parity, overrun, framing or break interrupt). - **The D16950 includes a programmable baud rate generator, which is capable to divide the timing reference clock input by divisors of 1 to (216-1) and produce a n × clock for driving the internal transmitter logic** – explains Jacek Hanke, DCD's CEO. **Provisions are also included to use this n × clock to drive the receiver logic**.

The D16950 UART IP Core is equipped with a complete MODEM-control capability and a processor-interrupt system. - **Interrupts can be programmed in accordance to your requirements, minimizing computing required to handle the communications link** – adds Hanke. The D16950 core includes all other UARTs (16450, 16550, 16650 and 16750) features and additional functions. Saying this, one can mention the ICR registers, which give additional capabilities of UART work configuration. The data transmission may be synchronized by an external clock connected to the RI (for receiver and transmitter) or the DSR (only for receiver) pin. The NMR register enables a 9-bit mode transmission, with or without special character. Writing and

Peripherals:

- HDLC/SDLC
- Smart Card Reader Unit
- EEPROM SPI Ctrl
- LCD Ctrl
- Floating Point Unit
- I2C Master/Slave
- SPI Master/Slave
- CAN bus
- LIN bus
- Programmable Peripheral Interface
- UART, UART with FIFO
- PWM
- Timer 8254
- Programmable Timer
- Interrupt Controller
- Ethernet Controller 10/100/1000 BaseT
- DMA Controller
- USB 1.0/2.0 Host/Salve
- On Chip Bus Analyzer

PCI Bus Controllers and Peripherals:

- PCI Express
- PCI-X Host Bridge Master/Target
- PCI Host Bridge Master/Target
- PCI-PCI Bridge
- PCI-ISA Bridge
- PCI Bus Arbiter

Modulation:

- ADPSM

AHB/APB Peripherals:

- AHB Bus Master/Slave

reading from/to FIFO may be controlled by trigger level registers, with any value set from 1 to 127.

DCD's IP Core implements also **auto flow control feature**, which can significantly reduce software overload and automatically increase the system efficiency, by controlling serial data flow through the RTS output and the CTS input signals.

The D16950 is perfect for applications, where the UART core and the microcontroller are clocked by the same clock signal and are implemented inside the same ASIC or FPGA chip. Nevertheless, it's also a proprietary solution for a standalone implementation, where several UARTs are required to be implemented inside a single chip and driven by some off-chip devices. Thanks to a universal inter-face, the D16950 core implementation and verification are very simple, just by eliminating a number of clock trees in the complete system.

DCD's IP Core includes fully automated test bench with complete set of tests, allowing easy package validation at each stage of SoC design flow. The D16950 is also a technology independent design, that can be implemented in a variety of process technologies.

D16950 Key Features:

- Software compatible with 16450, 16550,16650,16750 and 16950 UARTs
  - Configuration capability
  - Separate configurable BAUD clock line
  - Majority Voting Logic
  - Two modes of operation: UART mode and FIFO mode
    + In the FIFO mode transmitter and receiver are each buffered with 128 byte FIFO to reduce the number of interrupts presented to the CPU
    + In UART mode receiver and transmitter are double buffered to eliminate the need for precise synchro-nization between the CPU and serial data
  - Configurable FIFO size up to 512 levels
  - Adds or deletes standard asynchronous communication bits

- **APB Bus Master/Slave**
- **AHB/AXI DMA Controller**
- **AXI Bus Master/Slave**

MIPS CPU Interface:

- **MIPS - SysAD Bus Slave**
- **MIPS - SysAD Bus to PCI Host bridge**
- **MIPS - EC interface to SDRAM Controller**
- **MIPS - EC Interface to PCI Host Bridge**
- **MIPS - EC Interface Bus Slave**

PowerPC CPU Interface:

- **Power PC Bus Master**
- **PowerPC to PCI Host bridge**
- **PowerPC Bus Arbiter**
- **PowerPC Bus Slave**

ARC CPU Interface:

- **ARC - Peripheral Controller for ARCtangent**
- **ARC – ARCtangent to PCI host Bridge**

Contact us for data sheet

(start, stop and parity) to or from the serial data

- Independently controlled transmit, receive, line status and data set interrupts
- False start bit detection
- 16 bit programmable baud generator
- Independent receiver clock input
- MODEM control functions (CTS, RTS, DSR, DTR, RI, DCD)
- Programmable Hardware Flow Control through RTS and CTS
- Programmable Flow Control using DTR and DSR
- Programmable in-band Flow Control using XON/XOFF
- Programmable special characters detection
- Trigger levels for TX and RX FIFO
- Interrupts and automatic in-band and out-off-band flow control
- Fully programmable serial-interface characteristics:
  + 5-, 6-, 7-, 8- or 9-bit characters
  + Even, odd, or no-parity bit generation and detection
  + 1-, 1.5-, or 2-stop bit generation
  + Internal baud generator
- Detection of bad data in receiver FIFO
- Clock prescaler from 1 to 31,875
- Enhanced isochronous clock option
- 9- bit data mode
- Software reset
- Complete status reporting capabilities
- Line break generation and detection. Internal diagnostic capabilities:
  + Loop-back controls for communications link fault isolation
  + Break, parity, overrun, framing error simulation
- Full prioritized interrupt system controls
- Available system interface wrappers:

+ AMBA - APB Bus
+ Altera Avalon Bus
+ Xilinx OPB Bus

- Fully synthesizable
- Static synchronous design and no internal tri-states

We are looking forward to hear from you.

Contact us for more information.

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Until the next eNews,

Thanks you for your attention.

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