



KAL - Large IP Cores:

Analog IP Cores:

- Analog IP cores (ADC, DAC, PLL,) are available – Please contact us.
- We are expert in custom analog IP

CPU Cores:

- 32 bit - NEW
- 8 bit - 8051
- 8 bit- HC68HC11
- 8 bit - PIC Processor
- 8 bit – Z80
- 16 bit – D6800

Memory Controllers:

- SD/SDIO 2.0/3.0 Controller
- SDRAM Controller
- DDR/DDR2/DDR3 SDRAM Controller
- NAND Flash Controller
- Flash/EEPROM/SRAM Controller
- PCMCIA/CompactFlash Host Adapter
- PCMCIA/CompactFlash Slave Controller

Clock Synchronization:

- IEEE 1588 Slave
- IEEE 1588 Master
- IEEE 1588 Master/Slave
- IEEE 1588 PTP Stack
- IEEE 1588 L2/L3 Solution

Concept Engineering Presents Version 6 of All Debugging Tools for Analog, Digital, AMS and SoC Designers at DAC 2015

Concept Engineering, specialists in visualization and debugging technology for electronic circuits and systems, will demonstrate version 6 of the company's Vision product line to designers of analog, digital, mixed-signal circuits, systems-on-chip (SoCs), and field-programmable gate arrays (FPGAs) at the 52nd Design Automation Conference (DAC) in San Francisco, California, in June 2015.

StarVision® PRO, RTLvision® PRO, GateVision® PRO, and SpiceVision® PRO are customizable and scriptable debugging and visualization software tools that help electronic design engineers to easily understand, debug, optimize and document their designs. StarVision PRO provides analog, digital and mixed-signal debugging capabilities, customizable design rule checks and automated netlist pruning. RTLvision PRO is used for RTL debugging and intellectual property (IP) development. Designers use GateVision PRO for advanced netlist debugging of complex SoC netlists. SpiceVision PRO provides advanced exploration and debugging features for transistor-level and post-layout netlists. SpiceVision PRO's unique SPICE netlist visualization capabilities help engineers to analyze SPICE simulation results and allow easy location of circuit problems at the device level.

“With version 6, we continue to improve our specialized product family with individual tools for specific circuit debugging problems,” said Pascal Bolzhauser, product manager for Concept Engineering’s Vision product line. “We have made specific enhancements to each tool and we also have incorporated multiple general usability improvements.”

Notable enhancements in the version 6 platform are:

- Improved netlist pruning: In addition to Verilog and SPICE netlist export and pruning, StarVision PRO

Peripherals:

- HDLC/SDLC
- Smart Card Reader Unit
- EEPROM SPI Ctrl
- LCD Ctrl
- Floating Point Unit
- I2C Master/Slave
- SPI Master/Slave
- CAN bus
- LIN bus
- Programmable Peripheral Interface
- UART, UART with FIFO
- PWM
- Timer 8254
- Programmable Timer
- Interrupt Controller
- Ethernet Controller 10/100/1000 BaseT
- DMA Controller
- USB 1.0/2.0 Host/Slave
- On Chip Bus Analyzer

PCI Bus Controllers and Peripherals:

- PCI Express
- PCI-X Host Bridge Master/Target
- PCI Host Bridge Master/Target
- PCI-PCI Bridge
- PCI-ISA Bridge
- PCI Bus Arbiter

Modulation:

- ADPSM

AHB/APB Peripherals:

- AHB Bus Master/Slave

now also allows netlist pruning for the most common post-layout formats, DSPF and SPEF.

- Advanced post-layout debugging: Improved visualization and debugging of parasitic networks.

- API improvements: Improvements in the database API and GUI API allow even more sophisticated code to be developed and executed by the tool.

- Advanced batch processing: Enhanced batch processing capabilities allow more efficient processing of user-defined analysis and debugging tasks.

- Unified File Open Dialog: Makes it easier to load complex mixed-language SoC designs and libraries.

- Improved visual debugging capabilities such as: Smart connectivity lens view, improved schematic navigation history, and on-the-fly hierarchy exploration with built-in fold and un-fold controls.

The company's schematic generation tools for EDA tool developers and the new version 6 of the company's visualization and debugging tools will be demonstrated in the Concept Engineering booths (#2208 and 2210) at DAC 2015 in Moscone Center, San Francisco, from June 8th to June 10th, 2015.

Availability:

Version 6.0 products are available now to download from the company's website. There are no additional fees for existing customers with valid licenses.

About Concept Engineering:

Concept Engineering is a privately-held company based in Freiburg, Germany, that provides visualization and debugging technology for electronic circuits and systems, including automatic schematic generation technology for all major design levels. The company's technology helps electronic design engineers to easily understand, debug, optimize and document electronic designs. Concept Engineering's software technology is used in many fields in the EDA market, including: RTL development, IP reuse, ASIC and SoC design, FPGA design, analog/mixed-signal design, logic synthesis, design verification, test automation, post-layout analysis, debugging and visualization at system level, RTL level, netlist level and transistor level.

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- APB Bus Master/Slave
- AHB/AXI DMA Controller
- AXI Bus Master/Slave

MIPS CPU Interface:

- MIPS - SysAD Bus Slave
- MIPS - SysAD Bus to PCI Host bridge
- MIPS - EC interface to SDRAM Controller
- MIPS - EC Interface to PCI Host Bridge
- MIPS - EC Interface Bus Slave

PowerPC CPU Interface:

- Power PC Bus Master
- PowerPC to PCI Host bridge
- PowerPC Bus Arbiter
- PowerPC Bus Slave

ARC CPU Interface:

- ARC - Peripheral Controller for ARCTangent
- ARC – ARCTangent to PCI host Bridge

[Contact us for data sheet](#)

their respective owners.

We are looking forward to hear from you.

Contact us for more information.

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Until the next eNews,

Thanks you for your attention.

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