eNewsletter

**KAL - Large IP Cores:**

**Analog IP Cores:**

- **Analog IP cores (ADC, DAC, PLL,) are available – Please contact us.**
- **We are expert in custom analog IP**

**CPU Cores:**

- **8 bit - 8051**
- **8 bit- HC68HC11**
- **8 bit - PIC Processor**
- **8 bit – Z80**
- **16 bit – D6800**
- **DSP – MSP430**

**Memory Controllers:**

- **SD/SDIO 2.0/3.0 Controller**
- **SDRAM Controller**
- **DDR/DDR2/DDR3 SDRAM Controller**
- **NAND Flash Controller**
- **Flash/EEPROM/SRAM Controller**
- **PCMCIA/CompactFlash Host Adapter**
- **PCMCIA/CompactFlash Slave Controller**

**Clock Synchronization:**

- **IEEE 1588 Slave**
- **IEEE 1588 Master**
- **IEEE 1588 Master/Salve**
- **IEEE 1588 PTP Stack**
- **IEEE 1588 L2/L3 Solution**

# Concept Engineering Introduces S-engine™: Automatic System-Level Schematic Generation Capabilities Combined with IP Editing and Assembly

In 2010, Concept Engineering significantly improved transistor-level visualization for electronic design automation (EDA) tools in their NIView™ Widget platform with the introduction of T-engine™. This year, the company introduces S-engine™, which provides enhanced, automatic schematic generation that allows visualization at higher levels of abstraction. S-engine moves the Nlview Widget platform beyond visualization by providing smart editing capabilities at the system level, which makes it possible for developers to create tools for automated intellectual property (IP) and system-on-chip (SoC) assembly.

When integrated into high-level synthesis tools, S-engine provides excellent control over and visibility into the synthesis process. At the same time, S-engine's automatic schematic generation allows visualization at higher levels of abstraction, such as interface connections and intelligent IP-on-the-fly management, to easily handle configurable IP building blocks. Smart editing capabilities allow the creation of new and innovative SoC, network-on-chip (NoC) and IP design tools.

S-engine's combination of visualization and editing features enables system designers to rapidly instantiate, configure and connect the design elements that form complex SoCs. With support for higher levels of abstraction, S-engine can be used to create tools that visualize system descriptions derived from SystemC, SystemVerilog or other high-level description

**Peripherals:**

- **HDLC/SDLC**
- **Smart Card Reader Unit**
- **EEPROM SPI Ctrl**
- **LCD Ctrl**
- **Floating Point Unit**
- **I2C Master/Slave**
- **SPI Master/Slave**
- **CAN bus**
- **LIN bus**
- **Programmable Peripheral Interface**
- **UART, UART with FIFO**
- **PWM**
- **Timer 8254**
- **Programmable Timer**
- **Interrupt Controller**
- **Ethernet Controller 10/100/1000 BaseT**
- **DMA Controller**
- **USB 1.0/2.0 Host/Salve**
- **On Chip Bus Analyzer**

**PCI Bus Controllers and Peripherals:**

- **PCI Express**
- **PCI-X Host Bridge Master/Target**
- **PCI Host Bridge Master/Target**
- **PCI-PCI Bridge**
- **PCI-ISA Bridge**
- **PCI Bus Arbiter**

**Modulation:**

- **ADPSM**

**AHB/APB Peripherals:**

- **AHB Bus Master/Slave**

languages. For additional information, see the S-engine datasheet at http://www.concept.de/datasheet_sengine.pdf.

"As design complexity continues to grow and design teams use more and more in-house or third-party IP as part of their SoC, NoC or IP creation, the need for visualization and design technology at the IP level and system level becomes increasingly important," said Gerhard Angst, CEO and president of Concept Engineering. "Combining system-level schematic generation capabilities with IP editing and assembly features gives our customers exciting new options to create tools for system exploration and system definition."

## About Concept Engineering

Concept Engineering is a privately-held company based in Freiburg, Germany, that provides visualization and debugging technology for electronic circuits and systems, including automatic schematic generation technology for all major design levels. The company's technology helps electronic design engineers to easily understand, debug, optimize and document electronic designs. Concept Engineering's software technology is used in many fields in the EDA market, including: RTL development, IP reuse, ASIC and SoC design, FPGA design, analog/ mixed-signal design, logic synthesis, design verification, test automation, post-layout analysis, debugging and visualization at system level, RTL level, netlist level and transistor level.



We are looking forward to hear from you.

- **APB Bus Master/Slave**
- **AHB/AXI DMA Controller**
- **AXI Bus Master/Slave**

**MIPS CPU Interface:**

- **MIPS - SysAD Bus Slave**
- **MIPS - SysAD Bus to PCI Host bridge**
- **MIPS - EC interface to SDRAM Controller**
- **MIPS - EC Interface to PCI Host Bridge**
- **MIPS - EC Interface Bus Slave**

**PowerPC CPU Interface:**

- **Power PC Bus Master**
- **PowerPC to PCI Host bridge**
- **PowerPC Bus Arbiter**
- **PowerPC Bus Slave**

**ARC CPU Interface:**

- **ARC - Peripheral Controller for ARCtangent**
- **ARC – ARCtangent to PCI host Bridge**

**Contact us for data sheet**

Contact us for more information.

**Tel +972-4-6201129**

**Fax +972-4-6201328**

**www.KALtech.co.il**

info@kaltech.co.il

Facebook: kal silicon

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Until the next eNews,

Thanks you for your attention.

KAL

**Contact details:**

**Tel +972-4-6201129**

**Fax +972-4-6201328**

**www.KALtech.co.il**

info@kaltech.co.il

**eNews registration: http://www.kaltech.co.il/**