eNewsletter

KAL - Large IP Cores:

Analog IP Cores:

- **Analog IP cores (ADC, DAC, PLL,) are available – Please contact us.**
- **We are expert in custom analog IP**

CPU Cores:

- **8 bit - 8051**
- **8 bit - 80251**
- **8 bit- HC68HC11**
- **8 bit - PIC Processor**
- **8 bit – Z80**
- **16 bit – D6800**
- **DSP – MSP430**
- **32 bit - ARM 9xx/11xx**

Memory Controllers:

- **SD/SDIO 2.0/3.0 Controller**
- **SDRAM Controller**
- **DDR/DDR2/DDR3 SDRAM Controller**
- **NAND Flash Controller**
- **Flash/EEPROM/SRAM Controller**
- **PCMCIA/CompactFlash Host Adapter**
- **PCMCIA/CompactFlash Slave Controller**

Clock Synchronization:

- **IEEE 1588 Slave**
- **IEEE 1588 Master**
- **IEEE 1588 Master/Salve**

Concept Engineering Adds Support for Cadence® Virtuoso® Spectre® to StarVision™ PRO, SpiceVision® PRO and SGvisionTM PRO

Concept Engineering is adding Cadence® Virtuoso® Spectre® netlist support to its mixed-signal visualization and debugging tools, StarVision™ PRO, SpiceVision® PRO and SGvisionTM PRO. Adding support for another leading simulation netlist to the Spice formats that Concept already supports brings ultra fast design visualization and debugging as well as reduced development time to customers who use Spectre for circuit design and verification.

Concept Engineering's software tools help electronic design engineers to easily understand, debug, optimize, and document electronic designs. Concept's visualization and debugging tools already support important Spice formats such as Synopsys' HSPICE, Cadence's CDL, and Mentor's Eldo and Calibre as well as post-layout formats such as DSPF (detailed standard parasitic format). Support for the Spectre format extends Concept Engineering's support for mixed-signal design and accelerates product development for customers.

"Our leading microcontroller products are providing more and more advanced analog and mixed-signal features on-chip," said Nick Ayoub, Principal Staff Engineer, Microchip Technology Inc. "StarVision PRO allows full chip navigation of both digital and analog design descriptions at the same time in one single integrated design cockpit. Support for Spice and SystemVerilog netlist formats gives us even more options for future design projects."

Ori Galzur, vice president of design center and design enablement from TowerJazz Semiconductor added, "We provide our customers with a complex and unique set of library cells and StarVision PRO with its advanced schematic generation features enables us to quickly and automatically create schematic drawings for our mixedsignal libraries and PDKs. Support for the Spectre netlist format is a great additional input language and allows wider usage of the Concept Engineering tools within TowerJazz." "Hundreds of analog, digital, mixed-signal, RF and post-layout chip designers use Concept Engineering's StarVisionPRO, SpiceVision PRO and Sgvision PRO," said Gerhard Angst, CEO and president of Concept Engineering.

- **IEEE 1588 PTP Stack**
- **IEEE 1588 L2/L3 Solution**

Peripherals:

- **Floating Point Unit**
- **I2C Master/Slave**
- **SPI Master/Slave**
- **CAN bus**
- **LIN bus**
- **Programmable Peripheral Interface**
- **UART, UART with FIFO**
- **PWM**
- **Timer 8254**
- **Programmable Timer**
- **Interrupt Controller**
- **Ethernet Controller 10/100/1000 BaseT**
- **DMA Controller**
- **USB 1.0/2.0 Host/Salve**
- **On Chip Bus Analyzer**

PCI Bus Controllers and Peripherals:

- **PCI Express**
- **PCI-X Host Bridge Master/Target**
- **PCI Host Bridge Master/Target**
- **PCI-PCI Bridge**
- **PCI-ISA Bridge**
- **PCI Bus Arbiter**

Encryption:

- **AES 128bit/256bit**
- **ECC**

AHB/APB Peripherals:

- **AHB Bus Master/Slave**
- **APB Bus Master/Slave**

"Many of these customers have asked for Spectre support and we are happy to provide solutions to cover even more design formats and fit into more advanced mixed-signal debugging design and verification flows."

Pricing and availability:

Spectre netlist support will be part of SpiceVision PRO, StarVision PRO and SGvision PRO time-based licenses, with no additional license fees for customers already under license. Beta versions of the new products was demonstrated at DAC 2012; production is targeted for Q3 2012.

About Concept Engineering:

Concept Engineering is a privately held company based in Freiburg, Germany, founded in 1990 to develop and market innovative schematic generation and viewing technology for use with logic synthesis, verification, circuit characterization, circuit optimization, test automation and physical design tools. The company's customers are primarily EDA tool manufacturers (OEMs), in-house CAD tool developers and semiconductor companies.

-> Click here for Previews newsletter
-> Contact us for more information:

by phone: 04-6201129 Ext 4

by fax: 04-6201328

by email: info@kaltech.co.il

by Web: www.kaltech.co.il

by skype: adi_katav

by Facebook: kal silicon

Contact via LinkedIn http://www.linkedin.com/pub/adi-katav/30/b57/b1a

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Untill the next eNews,

Thanks yu for your attenstion.

KAL

- **AHB/AXI DMA Controller**
- **AXI Bus Master/Slave**

MIPS CPU Interface:

- **MIPS - SysAD Bus Slave**
- **MIPS - SysAD Bus to PCI Host bridge**
- **MIPS - EC interface to SDRAM Controller**
- **MIPS - EC Interface to PCI Host Bridge**
- **MIPS - EC Interface Bus Slave**

PowerPC CPU Interface:

- **Power PC Bus Master**
- **PowerPC to PCI Host bridge**
- **PowerPC Bus Arbiter**
- **PowerPC Bus Slave**

ARC CPU Interface:

- **ARC - Peripheral Controller for ARCtangent**
- **ARC – ARCtangent to PCI host Bridge**

Contact us for data sheet

Contact details:

Tel +972-4-6201129 Ext: 4

Fax +972-4-6201328

www.KALtech.co.il

info@kaltech.co.il

eNews registration: http://www.kaltech.co.il/