eNewsletter

KAL - Large IP Cores:

Analog IP Cores:

- **DDR2/3 PHY**
- **Analog IP cores (ADC, DAC, PLL,) are available – Please contact us.**
- **We are expert in custom analog IP**

CPU Cores:

- **8 bit - 8051**
- **8 bit- HC68HC11**
- **8 bit - PIC Processor**
- **8 bit – Z80**
- **16 bit – D6800**
- **DSP – MSP430**
- **32 bit - ARM 9xx/11xx**

Memory Controllers:

- **SD/SDIO 2.0/3.0 Controller**
- **SDRAM Controller**
- **DDR/DDR2/DDR3 SDRAM Controller**
- **NAND Flash Controller**
- **Flash/EEPROM/SRAM Controller**
- **PCMCIA/CompactFlash Host Adapter**
- **PCMCIA/CompactFlash Slave Controller**

Clock Synchronization:

- **IEEE 1588 Slave**
- **IEEE 1588 Master**

Our partner ICMASK Design form Ireland is professional for IC Training. The next training is RF Layout Techniques. and will be done in Dublin, Ireland on April 26th-29th 2011. Details are as follows. Contact us for more information.

RF Layout Techniques

The RF Physical Design course is targeted towards developing the skills necessary to complete the layout of an RF design. With a primary focus on CMOS processes, the course discusses the many challenges faced by RF CMOS layout and provides practical real life solutions.

COURSE CODE: RFLT01
COURSE PRE-REQUISITE: Prior experience of analog layout on a CMOS process
LEARNING OUTCOMES:

- Layout of RF circuits on CMOS processes
- Understanding of how layout influences circuit performance
- Schematic structure recognition and physical implementation

SYLLABUS CONTENT:

- Parasitics
  - Resistance and capacitance of interconnect
  - Inductance of interconnect
  - Device parasitics
- High speed MOS devices
  - Optimising device parasitics associated with MOS transistors
  - Unit fingers, donut devices, lattice structures
- Matching methodologies
  - Unit fingers, interleaving, common centroid, dummy insertion
- Shielding
  - Methodologies for shielding devices and interconnect from noise sources
- Substrate & Wells
  - Substrate model
  - Noise isolation techniques
  - Latch-up
- Supply considerations in RF designs
  - Isolation (natural decoupling)
  - Matched IR drop
  - Electromigration
- RF Components
  - Inductors
  - Varactor diodes
  - Flux capacitors

- **IEEE 1588 Master/Salve**
- **IEEE 1588 PTP Stack**
- **IEEE 1588 L2/L3 Solution**

Peripherals:

- **Floating Point Unit**
- **I2C Master/Slave**
- **SPI Master/Slave**
- **CAN bus**
- **LIN bus**
- **Programmable Peripheral Interface**
- **UART, UART with FIFO**
- **PWM**
- **Timer 8254**
- **Programmable Timer**
- **Interrupt Controller**
- **Ethernet Controller 10/100/1000 BaseT**
- **DMA Controller**
- **USB 1.0/2.0 Host/Salve**
- **On Chip Bus Analyzer**

PCI Bus Controllers and Peripherals:

- **PCI Express**
- **PCI-X Host Bridge Master/Target**
- **PCI Host Bridge Master/Target**
- **PCI-PCI Bridge**
- **PCI-ISA Bridge**
- **PCI Bus Arbiter**

Encryption:

- **AES 128bit/256bit**
- **ECC**

AHB/APB Peripherals:

- **AHB Bus Master/Slave**

Contact us for more information.

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Untill the next eNews,

Thanks yu for your attenstion.

KAL

- APB Bus Master/Slave
- AHB/AXI DMA Controller
- AXI Bus Master/Slave

MIPS CPU Interface:

- MIPS - SysAD Bus Slave
- MIPS - SysAD Bus to PCI Host bridge
- MIPS - EC interface to SDRAM Controller
- MIPS - EC Interface to PCI Host Bridge
- MIPS - EC Interface Bus Slave

PowerPC CPU Interface:

- Power PC Bus Master
- PowerPC to PCI Host bridge
- PowerPC Bus Arbiter
- PowerPC Bus Slave

ARC CPU Interface:

- ARC - Peripheral Controller for ARCtangent
- ARC – ARCtangent to PCI host Bridge

Contact us for data sheet

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