



KAL - Large IP Cores:

Analog IP Cores:

- Analog IP cores (ADC, DAC, PLL,) are available – Please contact us.
- We are expert in custom analog IP

CPU Cores:

- **8 bit - 8051**
- 8 bit- HC68HC11
- 8 bit - PIC Processor
- 8 bit – Z80
- 16 bit – D6800
- **DSP – MSP430**

Memory Controllers:

- **SD/SDIO 2.0/3.0 Controller**
- SDRAM Controller
- **DDR/DDR2/DDR3 SDRAM Controller**
- NAND Flash Controller
- Flash/EEPROM/SRAM Controller
- PCMCIA/CompactFlash Host Adapter
- PCMCIA/CompactFlash Slave Controller

Clock Synchronization:

- IEEE 1588 Slave
- IEEE 1588 Master
- IEEE 1588 Master/Salve
- IEEE 1588 PTP Stack
- IEEE 1588 L2/L3 Solution

Smart Card Reader IP Core

The DSMART is a fast, versatile and cost-competitive core intended for smart card reader applications. It provides a communication interface with a smart card, based on **ISO 7816-3/EMV4.2** requirements. DCD's IP Core implements the hardware support for both T0 character oriented protocol and T1 block oriented protocol. It's been designed to combine **highly reduced CPU utilization and low area consumption**, it is able to **activate and deactivate cards, perform resets, handle ATR reception and many additional features**. Configuration options enable user to adjust the

DSMART to his needs and choose the proprietary options, which will be the most suitable for his design. Data transfer to and from the host system can be interrupt-driven or executed through Direct Memory Access (DMA). The automatic convention detection and decoding mechanism ensure the **exact result** regardless of the used convention. Elementary Time Unit (ETU) - time duration of the one bit is decoded from the received ATR interface byte and generated automatically. The card clock divider provides non-gated clock with a wide range of possible frequencies. There's been also a **special power down mode** implemented, in which the card clock is being hold in two possible states, depending on the card parameter. Error signaling and character repetition are automatic for the T0 protocol. The DSMART incorporates also an optional **CRC/LRC hardware checking and generation mechanism** which gives the convention independent result. The received CRC/LRC is not stored in the FIFO, but can be read in a case of CRC/LRC error. Also the optional block length counter provides security of the DMA block transfer and automatic CRC/LRC, subjoining with a manual affixing option. The special block mode handles block transfer automatically. Status and error registers provide necessary information about the FIFO state, errors and card events.

Peripherals:

- HDLC/SDLC
- Smart Card Reader Unit
- Floating Point Unit
- I2C Master/Slave
- SPI Master/Slave
- CAN bus
- LIN bus
- Programmable Peripheral Interface
- UART, UART with FIFO
- PWM
- Timer 8254
- Programmable Timer
- Interrupt Controller
- Ethernet Controller 10/100/1000 BaseT
- DMA Controller
- USB 1.0/2.0 Host/Slave
- On Chip Bus Analyzer

PCI Bus Controllers and Peripherals:

- PCI Express
- PCI-X Host Bridge Master/Target
- PCI Host Bridge Master/Target
- PCI-PCI Bridge
- PCI-ISA Bridge
- PCI Bus Arbiter

Modulation:

- ADPSM

AHB/APB Peripherals:

- AHB Bus Master/Slave
- APB Bus Master/Slave
- AHB/AXI DMA Controller

* Note that DSMART works with all major CPUs and is 100% compatible with DCD's MCUs, enabling the same, cryptography.

We are looking forward to hear from you.

Contact us for more information.

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Until the next eNews,

Thanks you for your attention.

KAL

- AXI Bus Master/Slave

MIPS CPU Interface:

- MIPS - SysAD Bus Slave
- MIPS - SysAD Bus to PCI Host bridge
- MIPS - EC interface to SDRAM Controller
- MIPS - EC Interface to PCI Host Bridge
- MIPS - EC Interface Bus Slave

PowerPC CPU Interface:

- Power PC Bus Master
- PowerPC to PCI Host bridge
- PowerPC Bus Arbiter
- PowerPC Bus Slave

ARC CPU Interface:

- ARC - Peripheral Controller for ARCTangent
- ARC – ARCTangent to PCI host Bridge

[Contact us for data sheet](#)

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