



**KAL - Large IP Cores:**

Analog IP Cores:

- Analog IP cores (ADC, DAC, PLL,) are available – Please contact us.
- We are expert in custom analog IP

CPU Cores:

- **8 bit - 8051**
- 8 bit- HC68HC11
- 8 bit - PIC Processor
- 8 bit – Z80
- 16 bit – D6800
- **DSP – MSP430**

Memory Controllers:

- **SD/SDIO 2.0/3.0 Controller**
- SDRAM Controller
- DDR/DDR2/DDR3 SDRAM Controller
- NAND Flash Controller
- Flash/EEPROM/SRAM Controller
- PCMCIA/CompactFlash Host Adapter
- PCMCIA/CompactFlash Slave Controller

Clock Synchronization:

- IEEE 1588 Slave
- IEEE 1588 Master
- IEEE 1588 Master/Slave
- IEEE 1588 PTP Stack
- IEEE 1588 L2/L3 Solution

## LCD Controller IP Core

The DLCD is a display controller with 24-bit RGB output and synchronization. It may be used for displaying data, both on LCD and CRT displays. Pixel data has an 8-bit resolution and a 24-bit RGB output is generated using external LUT with defined color palette. Our "multimedial" Core is controlled by the CPU, which enables usage of external data memory to display data. All parameters are configurable through the CPU register interface. The core was designed to be used with DCD's DP80xxx series of MCU. The display controller is perfect for MCU based applications, where static graphic data is displayed using a LCD/TFT matrix or a CRT monitor. Our unique core is a technology independent design, that can be implemented in a variety of process technologies.

### Key Features

- Maximum resolution 1024 x 1024 pixels
  - 24-bit RGB output, 8-bit pixel with external LUT for color palette
  - Configurable screen parameters
  - Configurable memory data bus width
  - Wait states for memory access
  - Pixel clock divider

#### Peripherals:

- Smart Card Reader Unit
- Floating Point Unit
- I2C Master/Slave
- SPI Master/Slave
- CAN bus
- LIN bus
- Programmable Peripheral Interface
- UART, UART with FIFO
- PWM
- Timer 8254
- Programmable Timer
- Interrupt Controller
- Ethernet Controller 10/100/1000 BaseT
- DMA Controller
- USB 1.0/2.0 Host/Slave
- On Chip Bus Analyzer

#### PCI Bus Controllers and Peripherals:

- PCI Express
- PCI-X Host Bridge Master/Target
- PCI Host Bridge Master/Target
- PCI-PCI Bridge
- PCI-ISA Bridge
- PCI Bus Arbiter

#### Encryption:

- AES 128bit/256bit
- ECC

#### AHB/APB Peripherals:

- AHB Bus Master/Slave
- APB Bus Master/Slave
- AHB/AXI DMA Controller

- Display data copying without CPU access
- Display data accessible for CPU as external data memory
- Fully synthesizable
- Static synchronous design and no internal tri-states

### **Applications**

- Microcontroller based application
  - Displaying data on LCD/TFT matrix
  - Displaying data on LCD/TFT or CRT monitor

We are looking forward to hear from you.

Contact us for more information.

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Until the next eNews,

Thanks you for your attention.

KAL

- AXI Bus Master/Slave

MIPS CPU Interface:

- MIPS - SysAD Bus Slave
- MIPS - SysAD Bus to PCI Host bridge
- MIPS - EC interface to SDRAM Controller
- MIPS - EC Interface to PCI Host Bridge
- MIPS - EC Interface Bus Slave

PowerPC CPU Interface:

- Power PC Bus Master
- PowerPC to PCI Host bridge
- PowerPC Bus Arbiter
- PowerPC Bus Slave

ARC CPU Interface:

- ARC - Peripheral Controller for ARCTangent
- ARC – ARCTangent to PCI host Bridge

[Contact us for data sheet](#)

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