**KAL - Large IP Cores:**

**Analog IP Cores:**

- **Analog IP cores (ADC, DAC, PLL,) are available – Please contact us.**
- **We are expert in custom analog IP**

**CPU Cores:**

- **8 bit - 8051**
- **8 bit- HC68HC11**
- **8 bit - PIC Processor**
- **8 bit – Z80**
- **16 bit – D6800**
- **DSP – MSP430**

**Memory Controllers:**

- **SD/SDIO 2.0/3.0 Controller**
- **SDRAM Controller**
- **DDR/DDR2/DDR3 SDRAM Controller**
- **NAND Flash Controller**
- **Flash/EEPROM/SRAM Controller**
- **PCMCIA/CompactFlash Host Adapter**
- **PCMCIA/CompactFlash Slave Controller**

**Clock Synchronization:**

- **IEEE 1588 Slave**
- **IEEE 1588 Master**
- **IEEE 1588 Master/Salve**
- **IEEE 1588 PTP Stack**

# EEPROM IP Core with configurable SPI by DCD

*DEEPROM performs communication and exchanges data between external serial EEPROM Memory and CPU's RAM memory interface. Moreover, DCD's IP Core DEEPROM implements configurable SPI parameters like serial clock prescaler, SPI mode, CS hold/setup.*

Digital Core Design, celebrating in 2014 its 15th anniversary introduced newest IP Core which targets DRAM designs. The DEEPROM performs communication and exchanges data between external serial EEPROM Memory and CPU's RAM memory interface. Contents are accessible to the CPU in the same manner as a common SRAM memory, but require READY input to expand the time access. – Our proprietary core **allows to map serial EEPROM in processor memory space and control it as the parallel memory – says Jacek Hanke, DCD's CEO.**

The controller automatically sends all control instructions and read /write memory locations. As for the CPU, the EEPROM is being connected to it through the DEEPROM. Moreover, it's **visible and controlled as parallel SRAM with long access time. – DEEPROM's big advantage is that the** core has been **designed to operate with popular 25XXX SPI Serial EEPROMs** from Atmel, Microchip – adds Hanke.

- **IEEE 1588 L2/L3 Solution**

**Peripherals:**

- **HDLC/SDLC**
- **Smart Card Reader Unit**
- **Floating Point Unit**
- **I2C Master/Slave**
- **SPI Master/Slave**
- **CAN bus**
- **LIN bus**
- **Programmable Peripheral Interface**
- **UART, UART with FIFO**
- **PWM**
- **Timer 8254**
- **Programmable Timer**
- **Interrupt Controller**
- **Ethernet Controller 10/100/1000 BaseT**
- **DMA Controller**
- **USB 1.0/2.0 Host/Salve**
- **On Chip Bus Analyzer**

**PCI Bus Controllers and Peripherals:**

- **PCI Express**
- **PCI-X Host Bridge Master/Target**
- **PCI Host Bridge Master/Target**
- **PCI-PCI Bridge**
- **PCI-ISA Bridge**
- **PCI Bus Arbiter**

**Modulation:**

- **ADPSM**

**AHB/APB Peripherals:**

- **AHB Bus Master/Slave**
- **APB Bus Master/Slave**

When all other factors are sustained, memory controller is becoming crucial. That's why DCD's IP Core has been developed to ensure **the most accurate data flow**. It was designed in accordance with JEDEC specification and all the other industry standards, which summarized together make the DEEPROM **very small**, **efficient**, with no internal tri-state buffers and signals IP Core.

We are looking forward to hear from you.

Contact us for more information.

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Until the next eNews,

Thanks you for your attention.

KAL

- **AHB/AXI DMA Controller**
- **AXI Bus Master/Slave**

**MIPS CPU Interface:**

- **MIPS - SysAD Bus Slave**
- **MIPS - SysAD Bus to PCI Host bridge**
- **MIPS - EC interface to SDRAM Controller**
- **MIPS - EC Interface to PCI Host Bridge**
- **MIPS - EC Interface Bus Slave**

**PowerPC CPU Interface:**

- **Power PC Bus Master**
- **PowerPC to PCI Host bridge**
- **PowerPC Bus Arbiter**
- **PowerPC Bus Slave**

**ARC CPU Interface:**

- **ARC - Peripheral Controller for ARCtangent**
- **ARC – ARCtangent to PCI host Bridge**

**Contact us for data sheet**

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