



**KAL - Large IP Cores:**

Analog IP Cores:

- Analog IP cores (ADC, DAC, PLL,) are available – Please contact us.
- We are expert in custom analog IP

CPU Cores:

- **8 bit - 8051**
- 8 bit- HC68HC11
- 8 bit - PIC Processor
- 8 bit – Z80
- 16 bit – D6800

- **DSP – MSP430**

Memory Controllers:

- **SD/SDIO 2.0/3.0 Controller**
- SDRAM Controller
- DDR/DDR2/DDR3 SDRAM Controller
- NAND Flash Controller
- Flash/EEPROM/SRAM Controller
- PCMCIA/CompactFlash Host Adapter
- PCMCIA/CompactFlash Slave Controller

Clock Synchronization:

- IEEE 1588 Slave
- IEEE 1588 Master
- IEEE 1588 Master/Slave
- IEEE 1588 PTP Stack
- IEEE 1588 L2/L3 Solution

## ADPCM Controller IP Core By Oregano Systems

**The ADPCM (Adaptive Differential Pulse Code Modulation) algorithm performs speech compression of 64 kbit/s PCM data. The algorithm is standardized as ITU Standard G.721 and G.726.**

Fields of application range from classical voice based telecommunication (POTS) to industrial speech storage or speech output systems. The advantage of ADPCM is the comparable small computation effort required while delivering very good speech quality.

### Characteristics

Our parametrizable ADPCM IP core has been developed for usage in both ASIC as well as FPGA designs. The key features of the parametrizable ADPCM IP core are:

- very low resource requirements (gates/logic elements, memory)
- very small minimum clock frequency and thus a very small power consumption
- several parameters like number of channels, law encoding etc

**Peripherals:**

- Smart Card Reader Unit
- Floating Point Unit
- I2C Master/Slave
- SPI Master/Slave
- CAN bus
- LIN bus
- Programmable Peripheral Interface
- UART, UART with FIFO
- PWM
- Timer 8254
- Programmable Timer
- Interrupt Controller
- Ethernet Controller  
10/100/1000 BaseT
- DMA Controller
- USB 1.0/2.0 Host/Slave
- On Chip Bus Analyzer

**PCI Bus Controllers and Peripherals:**

- PCI Express
- PCI-X Host Bridge  
Master/Target
- PCI Host Bridge  
Master/Target
- PCI-PCI Bridge
- PCI-ISA Bridge
- PCI Bus Arbiter

**Modulation:**

- ADPCM

**AHB/APB Peripherals:**

- AHB Bus Master/Slave
- APB Bus Master/Slave
- AHB/AXI DMA Controller
- AXI Bus Master/Slave

We are looking forward to hear from you.

Contact us for more information.

**Tel +972-4-6201129**

**Fax +972-4-6201328**

**[www.KALtech.co.il](http://www.KALtech.co.il)**

**[info@kaltech.co.il](mailto:info@kaltech.co.il)**

Facebook: kal silicon

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Until the next eNews,

Thanks you for your attention.

KAL

MIPS CPU Interface:

- MIPS - SysAD Bus Slave
- MIPS - SysAD Bus to PCI Host bridge
- MIPS - EC interface to SDRAM Controller
- MIPS - EC Interface to PCI Host Bridge
- MIPS - EC Interface Bus Slave

PowerPC CPU Interface:

- Power PC Bus Master
- PowerPC to PCI Host bridge
- PowerPC Bus Arbiter
- PowerPC Bus Slave

ARC CPU Interface:

- ARC - Peripheral Controller for ARCTangent
- ARC – ARCTangent to PCI host Bridge

[Contact us for data sheet](#)

**Contact details:**

**Tel +972-4-6201129**

**Fax +972-4-6201328**

**[www.KALtech.co.il](http://www.KALtech.co.il)**

**[info@kaltech.co.il](mailto:info@kaltech.co.il)**

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