KAL - Large IP Cores:

Analog IP Cores:

- **Analog IP cores (ADC, DAC, PLL,) are available – Please contact us.**
- **We are expert in custom analog IP**

CPU Cores:

- **8 bit - 8051**
- **8 bit- HC68HC11**
- **8 bit - PIC Processor**
- **8 bit – Z80**
- **16 bit – D6800**
- **DSP – MSP430**

Memory Controllers:

- **SD/SDIO 2.0/3.0 Controller**
- **SDRAM Controller**
- **DDR/DDR2/DDR3 SDRAM Controller**
- **NAND Flash Controller**
- **Flash/EEPROM/SRAM Controller**
- **PCMCIA/CompactFlash Host Adapter**
- **PCMCIA/CompactFlash Slave Controller**

Clock Synchronization:

- **IEEE 1588 Slave**
- **IEEE 1588 Master**
- **IEEE 1588 Master/Salve**
- **IEEE 1588 PTP Stack**

Let me present you DCD's Product of the Month. The DLIN, our lucky winner, is a Local Interconnect Network soft core, fully **compatible with LIN 1.3, 2.1 and the newest 2.2. revision A**. It supports transmission speed between 1 and 20kb/s, being able to work as **a master or as a slave LIN node**, depending on a working mode determined by the CPU/MCU.
More technical details you can find in the following articles. Please don't forget that as for the Product of the Month, you can get the DLIN with 50% discounted license fee. And remember that February is short...

DLIN = Local Interconnect Network

The DLIN is the newest Local Interconnect Network IP Core developed by Digital Core Design. Polish IP Core provider has presented a solution, which is fully compatible with the LIN 1.3, 2.1 and the newest version 2.2 Revision A, released by the LIN Consortium. The core is described at RTL level, empowering the target use in both, FPGA and ASIC technologies.

The DLIN, DCD's IP Core for Local Interconnect Network, is an ideal solution most of all for automotive designs. As technologies and facilities implemented in a car grow every year, the need for a cheap serial network has arisen. That's why LIN seems to be the most suitable solution to integrate intelligent sensor devices or actuators in today's cars. Contrary to the CAN, it enables cost competitive serial communication, building the same an extended vehicle's electrical network, which... will be used as CAN's sub- network. - ***Our DLIN controller supports transmission speed between 1 and 20kb/s*** - says Jacek Hanke, CEO in Digital Core Design - ***that allows to transmit and receive LIN messages compatible to LIN 1.3, LIN 2.1 and also the newest LIN 2.2 rev A.***
Compared to the CAN, LIN is slower, but thanks to its simplicity, it is much more cost effective. That's why the DLIN is ideal for communication in

- **IEEE 1588 L2/L3 Solution**

Peripherals:

- **Floating Point Unit**
- **I2C Master/Slave**
- **SPI Master/Slave**
- **CAN bus**
- **LIN bus**
- **Programmable Peripheral Interface**
- **UART, UART with FIFO**
- **PWM**
- **Timer 8254**
- **Programmable Timer**
- **Interrupt Controller**
- **Ethernet Controller 10/100/1000 BaseT**
- **DMA Controller**
- **USB 1.0/2.0 Host/Salve**
- **On Chip Bus Analyzer**

PCI Bus Controllers and Peripherals:

- **PCI Express**
- **PCI-X Host Bridge Master/Target**
- **PCI Host Bridge Master/Target**
- **PCI-PCI Bridge**
- **PCI-ISA Bridge**
- **PCI Bus Arbiter**

Encryption:

- **AES 128bit/256bit**
- **ECC**

AHB/APB Peripherals:

- **AHB Bus Master/Slave**
- **APB Bus Master/Slave**
- **AHB/AXI DMA Controller**

intelligent sensors and actuators, where the bandwidth and versatility of CAN is not required. DCD's IP Core provides an interface between a microprocessor/microcontroller and a LIN bus. It can work as a master or as a slave LIN node, depending on a working mode determined by the CPU/MCU.

The reported information status includes the type and condition of transfer operations being performed by the DLIN, as well as a wide range of LIN error conditions (overrun, framing, parity, timeout). DCD's IP Core includes also a programmable timer, which allows to detect timeout and synchronization error. The Core is described at RTL level, empowering the target use in FPGA and ASIC technologies.

We are looking forward to hear from you.

Contact us for more information.

Tel +972-4-6201129 Ext: 4

Fax +972-4-6201328

www.KALtech.co.il

info@kaltech.co.il

Facebook: kal silicon

Until the next eNews,

Thanks you for your attention.

KAL

- **AXI Bus Master/Slave**

MIPS CPU Interface:

- **MIPS - SysAD Bus Slave**
- **MIPS - SysAD Bus to PCI Host bridge**
- **MIPS - EC interface to SDRAM Controller**
- **MIPS - EC Interface to PCI Host Bridge**
- **MIPS - EC Interface Bus Slave**

PowerPC CPU Interface:

- **Power PC Bus Master**
- **PowerPC to PCI Host bridge**
- **PowerPC Bus Arbiter**
- **PowerPC Bus Slave**

ARC CPU Interface:

- **ARC - Peripheral Controller for ARCtangent**
- **ARC – ARCtangent to PCI host Bridge**

Contact us for data sheet

Contact details:

Tel +972-4-6201129 Ext: 4

Fax +972-4-6201328

www.KALtech.co.il

info@kaltech.co.il

eNews registration: http://www.kaltech.co.il/