

KAL - Large IP Cores:

Analog IP Cores:

- Analog IP cores (ADC, DAC, PLL,) are available – Please contact us.
- We are expert in custom analog IP

CPU Cores:

- **8 bit - 8051**
- 8 bit- HC68HC11
- 8 bit - PIC Processor
- 8 bit – Z80
- 16 bit – D6800
- **DSP – MSP430**

Memory Controllers:

- **SD/SDIO 2.0/3.0 Controller**
- SDRAM Controller
- **DDR/DDR2/DDR3 SDRAM Controller**
- NAND Flash Controller
- Flash/EEPROM/SRAM Controller
- PCMCIA/CompactFlash Host Adapter
- PCMCIA/CompactFlash Slave Controller

Clock Synchronization:

- IEEE 1588 Slave
- IEEE 1588 Master
- IEEE 1588 Master/Salve
- IEEE 1588 PTP Stack
- IEEE 1588 L2/L3 Solution

DT8051 - the world's most powerful tiny 8051

Digital Core Design, IP Core provider and a System on Chip design house, has introduced the DT8051. It's the world's most powerful tiny 8051 available on the market. The complete system with peripherals and the DoCD™ debugger needs just 6 650 ASIC gates, when a standalone CPU utilizes little else than 3k gates.

The DT8051 is an area optimized tiny soft core of a single chip 8-bit embedded microcontroller, based on the most popular 8051 MCU. The Polish IP Core seems to be an excellent solution, also regarding to 32-bit ARM Cores, when even a plain Mo utilize more than 10000 gates. – *In terms of the cost & area of silicon-proven DT8051, not just other 8-bit MCUs, but also a 32-bit processor licensing comes close* – says Tomek Krzyzak, the Vice President of Digital Core Design. *Moreover, our DT8051 can run in very small FPGA devices or can be just a tiny fragment of a System-on-Chip ASIC - as the old saying goes: small is beautiful.* A very low gate count area allows as well running the core at high performance, up to 300 MHz in Hynix 0.18 library (equivalent performance to the original 80C51, clocked with 2400 MHz).



The DT8051 soft core is 100% binary-compatible with the industry standard 8051 8-bit microcontroller, but in comparison to its ancestor, DCD's IP Core has 8 times higher performance. It also offers a very low gate count architecture, giving 6 650 ASIC gates for the complete system with peripherals and the DoCD™ on-chip debugger. But the size wouldn't mean anything, without an appropriate performance. – *The DT8051 could be named a "mighty power"* – says Piotr Kandora, a VP & Director of R&D at DCD. *Dhrystone 2.1 benchmark program runs*

Peripherals:

- Floating Point Unit
- I2C Master/Slave
- SPI Master/Slave
- CAN bus
- LIN bus
- Programmable Peripheral Interface
- UART, UART with FIFO
- PWM
- Timer 8254
- Programmable Timer
- Interrupt Controller
- Ethernet Controller 10/100/1000 BaseT
- DMA Controller
- USB 1.0/2.0 Host/Slave
- On Chip Bus Analyzer

PCI Bus Controllers and Peripherals:

- PCI Express
- PCI-X Host Bridge Master/Target
- PCI Host Bridge Master/Target
- PCI-PCI Bridge
- PCI-ISA Bridge
- PCI Bus Arbiter

Encryption:

- AES 128bit/256bit
- ECC

AHB/APB Peripherals:

- AHB Bus Master/Slave
- APB Bus Master/Slave
- AHB/AXI DMA Controller
- AXI Bus Master/Slave

exactly 8.1 times faster, than the original 80C51 at the same frequency. The performance results are more than 2 times higher than the nearest competitive designs.

The DT8051 includes a 2-wire DoCD™ on-chip debugger (TTAG), up to eight external interrupt sources, an advanced Power Management Unit, Timers 0&1, I/O bit addressable Ports, full duplex UART and interface for external SFR. Furthermore, DCD's IP Core has a built-in support for the 2-wire TTAG interface - DCD Hardware Debug System, popular DoCD™. This version of the debugger is dedicated for applications, where a number of external pins is limited.

The DT8051 is delivered with fully automated test bench and complete set of tests, allowing easy package validation, at each stage of SoC design flow.

We are looking forward to hear from you.

Contact us for more information.

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Until the next eNews,

Thanks you for your attention.

KAL

MIPS CPU Interface:

- MIPS - SysAD Bus Slave
- MIPS - SysAD Bus to PCI Host bridge
- MIPS - EC interface to SDRAM Controller
- MIPS - EC Interface to PCI Host Bridge
- MIPS - EC Interface Bus Slave

PowerPC CPU Interface:

- Power PC Bus Master
- PowerPC to PCI Host bridge
- PowerPC Bus Arbiter
- PowerPC Bus Slave

ARC CPU Interface:

- ARC - Peripheral Controller for ARCTangent
- ARC – ARCTangent to PCI host Bridge

[Contact us for data sheet](#)

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