IP Cores Offering by KAL's Partners:

The combination of leading ASIC knowledge and customer ASIC project that we have done and doing in present, leading us to look for and to partnered with the leading IP vendors. Our Vendors offering leading IP for SOC (System-On-Chip) design for high speed performance, low power demand and small foot print.

Digital IP cores:

CPU Cores:

- 8 bit - 8051,
- 8 bit - 8051 Pipelined
- 8 bit - 8051 Quad-Pipelined Ultra High Performance
- 8 bit - PIC Processor
- 8 bit- HC68HC11
- 8 bit - 8051, 8051 Pipelined
- 8 bit – Z80
- 16 bit – D6800
- 16 bit DSP – MSP430

Memory Controllers:

- DDR2/DDR3 Controller
- LPDDR Controller
- SDRAM DIMM Controller
- SD/SDIO 2.0/3.0 Controller – eMMC support
- SDRAM Controller
- NAND Flash Controller
- Flash/EEPROM/SRAM Controller
- PCMCIA/CompactFlash Host Adapter
- PCMCIA/CompactFlash Slave Controller
- *Single/Multiport AHB/AXI/Other to all controllers*

Peripherals:

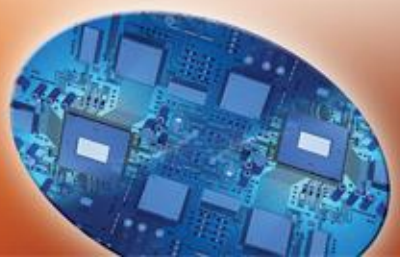
- Floating Point Unit
- I2C Master/Slave
- SPI Master/Slave
- CAN bus
- LIN bus
- Programmable Peripheral Interface
- UART, UART with FIFO
- PWM
- Timer 8254
- Programmable Timer
- Interrupt Controller
- 10/100/1000 Ethernet Controller
- DMA Controller

USB Controllers:

- USB 2.0/1.1 Device Controller
- USB 2.0/1.1 Host Controller
- USB 2.0/1.1 Hub Controller
- USB 2.0 On-The-Go
- USB Verification
- OTG Stack
- UTMI + to UTMI+ wrapper
- UTMI + to ULPI + wrapper
- Bus Socket Analyzer for OCP

Clock Synchronization:

- IEEE 1588 Slave
- IEEE 1588 Master
- IEEE 1588 Master/Salve
- IEEE 1588 PTP Stack
- IEEE 1588 L2/L3 Solution



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MIPS CPU Interface:

- MIPS - SysAD Bus Slave
- MIPS - SysAD Bus to PCI Host bridge
- MIPS - EC interface to SDRAM Controller
- MIPS - EC Interface to PCI Host Bridge
- MIPS - EC Interface Bus Slave

AHB Peripherals:

- AHB Bus Master/Slave
- APB Bus Master/Slave
- AHB/AXI DMA Controller
- AXI Bus Master/Slave

PCI Bus Controllers and Peripherals:

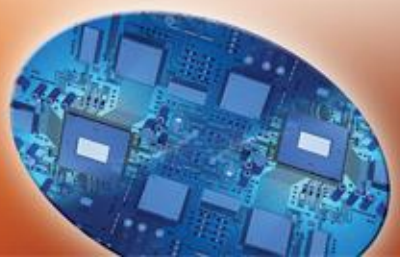
- PCI Express
- PCI-X Host Bridge, Master/Target
- PCI Host Bridge, Target, Master/Target
- PCI-PCI Bridge
- PCI-ISA Bridge
- PCI Bus Arbiter

PowerPC CPU Interface:

- Power PC Bus Master
- PowerPC to PCI Host bridge
- PowerPC Bus Arbiter
- PowerPC Bus Slave

ARC CPU Interface:

- ARC - Peripheral Controller for ARCtangent
- ARC – ARCtangent to PCI host Bridge



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Analog IP cores:

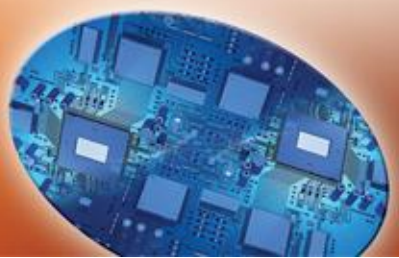
ADC

Architecture	Resolution	Sample Rate	Technology	Comments
ΣΔ ADC	14 Bit	1 KS/s	0.18µm	2nd Order Modulator @4MHz
ΣΔ ADC	12 Bit	12 KS/s	0.18µm	2-1 MASH Modulator @12MHz
ΣΔ ADC	14 Bit 12 Bit	10 MS/s 10 MS/s	0.18µm	2-1 MASH Modulator @64MHz @ 8KHz Bandwidth @ 500KHz Bandwidth
ΣΔ ADC	10 Bit	250 KS/s	0.18µm	1st Order Modulator @32MHz
SAR ADC	12 Bit	1 MS/s	0.18µm	C based
SAR ADC	10 Bit	1 MS/s	0.18µm	R based
ΣΔ ADC	13 Bit	1 MS/s	0.13µm	2-1-1 MASH Modulator @64MHz @ 500KHz Bandwidth

DAC

Architecture	Resolution	Sample Rate	Technology	Comments
RDAC	8 Bit	5 MS/s	0.18µm	
RDAC	10 Bit	1 MS/s	0.18µm	
ΣΔ DAC	12 Bit	1 MS/s	0.13µm	

We are specialized in noon standard analog IP, custom made per the customer specification. 0.35u – 40nm.



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