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Introducing the DP8051CPU of DCD

The DP8051CPU is an ultra high performance, speed optimized soft core of a single-chip 8-bit embedded controller dedicated for operation with fast (typically on-chip) and slow (off-chip) memories. The core has been designed with a special concern about performance to power consumption ratio. This ratio is extended by an advanced power management unit PMU.

The DP8051CPU soft core is 100% binary-compatible with the industry standard 8051 8-bit microcontroller. There are two configurations of DP8051CPU: Harvard where internal data and program buses are separated and von Neumann with common program and external data bus. The DP8051CPU has a Pipelined RISC architecture 10 times faster compared to standard architecture and executes 85-200 million instructions per second. This performance can also be exploited to great advantage in low power applications where the core can be clocked over ten times slower than the original implementation, without performance depletion.

The DP8051CPU is delivered with fully automated testbench and complete set of tests allowing easy package validation at each stage of SoC design flow. Each of the DCD's 8051 Core has built in support for DCD Hardware Debug System called DoCD™.

It is a real-time hardware debugger which provides debugging capability of a whole System on Chip (SoC). In contrast to other on-chip debuggers the DoCD™ provides non-intrusive debugging of running application. It can halt, run, step into or skip an instruction, read/write any contents of microcontroller including all registers, internal, external, program memories, all SFRs including user defined peripherals.